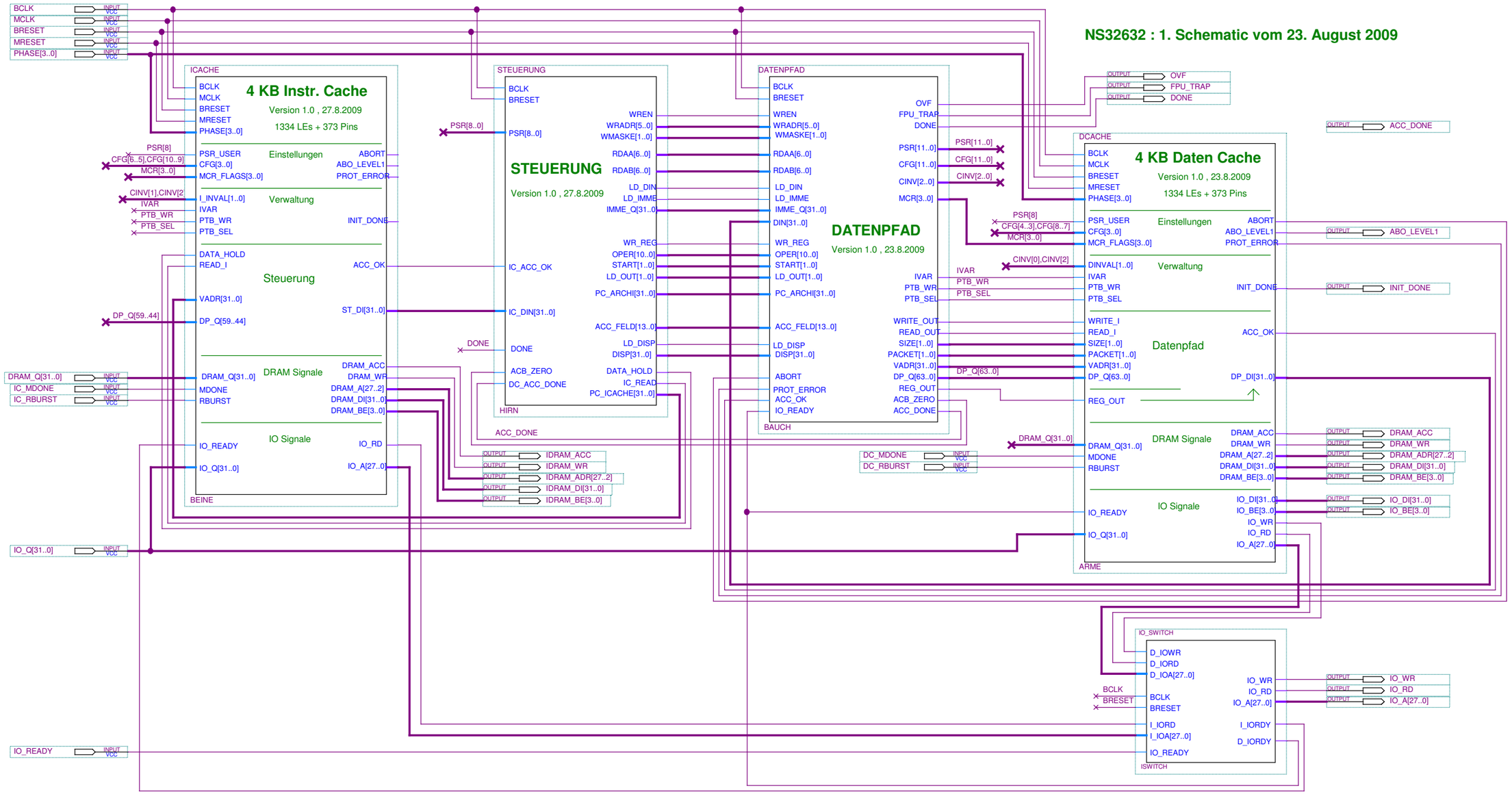
NS32632 : 1. Schematic vom 23. August 2009
ICACHE
4 KB Instr. Cache
Version 1.0 , 27.8.2009
1334 LEs + 373 Pins
Einstellungen
Verwaltung
Steuerung
DRAM Signale
IO Signale
BEINE
STEUERUNG
Version 1.0 , 27.8.2009
HIRN
DATENPFAD
Version 1.0 , 23.8.2009
BAUCH
DCACHE
4 KB Daten Cache
Version 1.0 , 23.8.2009
1334 LEs + 373 Pins
Datenpfad
ARME
IO_SWITCH
ISWITCH
BCLK
MCLK
BRESET
MRESET
PHASE[3..0]
DRAM_Q[31..0]
IC_MDONE
IC_RBURST
IO_Q[31..0]
IO_READY
DC_MDONE
DC_RBURST
OVF
FPU_TRAP
DONE
ACC_DONE
ABO_LEVEL1
INIT_DONE
IDRAM_ACC
IDRAM_WR
IDRAM_ADR[27..2]
IDRAM_DI[31..0]
IDRAM_BE[3..0]
DRAM_ACC
DRAM_WR
DRAM_ADR[27..2]
DRAM_DI[31..0]
DRAM_BE[3..0]
IO_DI[31..0]
IO_BE[3..0]
IO_WR
IO_RD
IO_A[27..0]